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Serial No. 10/090,806

September 5, 2003

Reply to the Office Action dated June 5, 2003

Page 6 of 10

REMARKS/ARGUMENTS

Claims 9-20 are pending in this application.

Claims 9-11 and 14 were rejected under 35 U.S.C. § 102(b) as being anticipated by Person et al. (5,321,573). Claims 12 and 13 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Person et al. in view of Nagakubo et al. (5,966,938). Claims 15-17 and 20 were rejected under 35 U.S.C. 103(a) as being unpatentable over Person et al. Claims 18 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Person in view of Nagakubo et al. Applicants respectfully traverse the rejections of claims 9-20.

Claim 9 recites:

“A manufacturing method of a chip-type composite electronic component comprising the steps of:
forming an inductor characteristic sheet by laminating a ceramic layer having an internal coil conductor;
forming a thermistor characteristic sheet by laminating a ceramic layer having an internal electrode and having a predetermined resistance-temperature characteristic;
forming a compound multilayer body by adhering the inductor characteristic sheet and the thermistor characteristic sheet by pressure with a diffusion-prevention layer sandwiched therebetween;
baking a compound multilayer body;
forming external electrodes on an end surface of a compound multilayer body in which at least one end part of an internal coil conductor and at least one end part of an internal electrode are exposed.” (emphasis added)

Claim 15 recites:

“A manufacturing method of a chip-type composite electronic component comprising the steps of:
forming an inductor characteristic sheet by laminating a ceramic layer having an internal coil conductor;
baking the inductor characteristic sheet;
forming a thermistor characteristic sheet by laminating a ceramic layer having an internal electrode and having a predetermined resistance-temperature characteristic;
baking the thermistor characteristic sheet;

Serial No. 10/090,806
September 5, 2003
Reply to the Office Action dated June 5, 2003
Page 7 of 10

forming a compound multilayer body by adhering and laminating the baked inductor characteristic sheet and the baked thermistor characteristic sheet;

forming external electrodes on an end surface of the compound multilayer body, in which at least one end part of an internal coil conductor and at least one end of an internal electrode are exposed." (emphasis added)

Applicants' claim 9 recites the step of "forming a compound multilayer body by adhering the inductor characteristic sheet and the thermistor characteristic sheet by pressure with a diffusion-prevention layer sandwiched therebetween." Applicants' claim 15 recites the step of "forming a compound multilayer body by adhering and laminating the baked inductor characteristic sheet and the baked thermistor characteristic sheet." With the improved features of claims 9 and 15, Applicants have been able to provide a method of manufacturing a small-sized chip-type composite electronic component in which the impedance can be changed depending on the temperature (see, for example, the last full paragraph on page 1 of the Specification).

The Examiner has alleged in the paragraph bridging pages 2 and 3 of the outstanding Office Action that Person et al. teaches the step of "forming a compound multilayer body by adhering the inductor characteristic sheet and the thermistor characteristic sheet by pressure (el. 12; col. 7 line 28 - col. 8 line 16) with a diffusion prevention layer sandwiched therebetween (el. 40; col. 3 lines 52-56)."

However, neither line 28 of column 7 to line 16 of column 8 of Person et al. nor lines 52-56 of column 3 of Person et al. teaches or suggests the feature of a "diffusion prevention layer" as recited in Applicants' claim 9. Line 28 of column 7 to line 16 of column 8 of Person et al. are directed to claims 11 and 12 of Person et al. which fail to recite any feature which corresponds to the feature of a "diffusion prevention layer" as recited in Applicants' claim 9.

Lines 52-56 of column 3 of Person et al. also fails to teach or suggest the feature of a "diffusion prevention layer" as recited in Applicants' claim 9. Person et al.

Serial No. 10/090,806

September 5, 2003

Reply to the Office Action dated June 5, 2003

Page 8 of 10

specifically discloses that element 40 (referred to by the Examiner) is a ferrite layer, **NOT** a diffusion prevention layer as recited in the present claimed invention. There is absolutely no hint or suggestion by Person et al. that ferrite layer 40 constitutes to a "diffusion prevention layer" as recited in Applicants' claim 9.

Thus, contrary to the Examiner's allegation, Person et al. clearly fails to teach or suggest the step of "forming a compound multilayer body by adhering the inductor characteristic sheet and the thermistor characteristic sheet by pressure with a diffusion-prevention layer sandwiched therebetween" (emphasis added) as recited in Applicants' claim 9.

Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 9 under 35 U.S.C. § 102(b) as being anticipated by Person et al.

The Examiner has relied upon Nagakubo et al. to cure various deficiencies in Person et al. However, Nagakubo et al. fails to teach or suggest the step of "forming a compound multilayer body by adhering the inductor characteristic sheet and the thermistor characteristic sheet by pressure with a diffusion-prevention layer sandwiched therebetween" as recited in Applicants' claim 9.

Applicants agree with the Examiner that Person et al. fails to teach or suggest the step of "forming a compound multilayer body by adhering and laminating the baked inductor characteristic sheet and the baked thermistor characteristic sheet."

The Examiner has alleged in the paragraph bridging pages 4 and 5 of the outstanding Office Action that "[i]t would have been obvious to a person skilled in the art at the time of the invention to perform and bake the thermistor and inductor sheets separately, then adhere and laminate them together in order to vary the electrical properties of the final device and [to] achieve the desired properties using preformed subassemblies (Person [et al.] - col.3 lines 42-51)."

First, the Examiner is reminded that prior art rejections must be based on evidence. Graham v. John Deere Co., 383 U.S. 117 (1966). The Examiner is hereby requested to cite a reference in support of his position that it was well known at the time

Serial No. 10/090,806
September 5, 2003
Reply to the Office Action dated June 5, 2003
Page 9 of 10

of Applicants' invention to "to perform and bake the thermistor and inductor sheets separately, then adhere and laminate them together." If the rejection is based on facts within the personal knowledge of the Examiner, the data should be supported as specifically as possible and the rejection must be supported by an affidavit from the Examiner, which would be subject to contradiction or explanation by affidavit of Applicants or other persons. See 37 C.F.R. § 1.104(d)(2).

Second, the Examiner has failed to explain why the motivations to vary the electrical properties of the final device would specifically lead one of any skill in the art "to preform and bake the thermistor and inductor sheets separately, then adhere and laminate them together." Lines 42-51 of Person et al. relied upon by the Examiner teach that additional layers 32, 34, and 36 maybe added to the varistor 24 to alter the varistor's electrical properties. However, neither the portion relied upon by the Examiner nor any other portion of Person et al. teaches or suggests that the step of preforming and baking the thermistor and inductor sheets separately and then adhering and laminating them together would alter the electrical properties of the varistor.

Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claim 15 under 35 U.S.C. 103(a) as being unpatentable over Person et al.

Accordingly, Applicants respectfully submit that Person et al. and Nagakubo et al., applied alone or in combination, fail to teach or suggest the unique combination and arrangement of elements recited in claims 9 and 15 of the present application. Claims 10-14 depend upon claim 9 and are therefore allowable for at least the reasons that claim 9 is allowable. Claims 16-20 depend upon claim 15 and are therefore allowable for at least the reasons that claim 15 is allowable.

In view of the foregoing amendments and remarks, Applicants respectfully submit that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

Serial No. 10/090,806
September 5, 2003
Reply to the Office Action dated June 5, 2003
Page 10 of 10

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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